REMARKS

Reconsideration of the present application is respectfully requested. Claims 1-26 previously presented for examination remain in the application. Claims 1, 11, 13, 18 and 19 have been amended to more clearly and distinctly claim the features that applicants regard as the invention and to place the claims in better form for consideration on appeal. No claims have been canceled or added.

Claims 1-26 stand rejected under 35 U.S.C. § 103(a) as being considered to be unpatentable over U.S. Patent No. 6,085,263 to Sharma et al. ("Sharma") in view of U.S. Patent No. 6,058,461 to Lewchuk ("Lewchuk").

Claim 1 includes the limitations

> a prefetch engine to prefetch data from a distributed, coherent memory in response to a first transaction from an input/output bus directed to the distributed, coherent memory; and
>
> an input/output coherent cache buffer to receive the prefetched data, the coherent cache buffer being coherent with the distributed, coherent memory and with other cache memories in a system including the input/output coherent cache buffer,
>
> the prefetch engine further to speculatively prefetch data in anticipation of a need for the speculatively prefetched data in association with a second input/output transaction if data has been prefetched for pending, memory-related transactions from the input/output bus.

(Claim 1)(emphasis added).

As previously argued and as admitted in the present Office Action, Sharma does not teach or suggest at least speculatively prefetching data as set forth in claim 1. The combination of Lewchuk with Sharma, were such a

combination to be made, would also fail to teach or suggest the claimed features of applicants' invention including at least the prefetch engine of claim 1 that speculatively prefetches data in anticipation of a need for the data in association with an input/output transaction.

As discussed previously, Sharma discloses a method and apparatus for employing commit-signals and prefetching to maintain inter-reference ordering in a high-performance I/O processor. In accordance with Sharma, a retire controller imposes inter-reference ordering among the operations based on receipt of a commit signal for each operation, wherein the commit signal for a memory reference operation indicates the apparent completion of the operation rather than actual completion of the operation. A prefetch controller coupled to an I/O cache prefetches data into a cache without any ordering constraints. The ordered retirement functions of the I/O processor are separate from its prefetching operations. (Sharma, Abstract).

Lewchuk discloses a computer system including priorities for memory operations that provides for higher priority memory operations to interrupt lower priority memory operations. According to Lewchuk, microprocessors assign a priority level to each memory operation as the memory operations are initiated. The priority levels may include a fetch priority level and a prefetch priority level. For some aspects of Lewchuk, speculative memory operations may be prioritized lower than non-speculative memory operations. (Lewchuk, e.g. Abstract).

Applicants respectfully submit that one of ordinary skill in the art would not have been motivated to combine Lewchuk with Sharma. Sharma relates to a

system in which a prefetch controller is coupled to an I/O cache for prefetching data into the cache without any ordering constraints. In contrast, Lewchuk relates to assigning priority levels to fetch and prefetch operations such that a higher priority operation may interrupt a lower priority operation.

Even if such a combination were to be made, however, applicants respectfully submit that the combination of Lewchuk with Sharma would still not lead one of ordinary skill in the art to arrive at the claimed invention.

It is stated in the Office Action that Lewchuk teaches speculatively prefetching as set forth in claim 1. Applicants respectfully disagree. The speculative memory operations disclosed by Lewchuk are related to speculative execution of instructions (see e.g. col. 6, lines 30-35) and not to I/O transactions. Lewchuk does not teach or suggest speculatively prefetching data in anticipation of an upcoming input/output transaction as set forth in claim 1.

For at least these reasons, claim 1 is patentably distinguished over the Sharma reference alone or in combination with Lewchuk.

Independent claims 11 and 19 include limitations similar to that discussed above in reference to claim 1. Claims 2-10, claims 12-18 and claims 20-26 depend from and further limit claims 1, 11 and 19. Thus, for at least the same reasons, claims 2-26 are patentably distinguished over the Sharma and Lewchuk references alone or in combination.

Based on the foregoing, applicants respectfully submit that the applicable rejections and objections have been overcome and that claims 1-26 are in condition for allowance. If the examiner disagrees or believes that further

discussion will expedite prosecution of this case, the examiner is invited to telephone applicants' representative at the number indicated below.

If there are any charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

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